Hybrid-Switched-Capacitor VRM with Zero-Voltage-Switching Intermediate Voltage Rails

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***Abstract*—The paper presents a novel hybrid-switched-capacitor voltage regulator module (HSC-VRM) design with Zero-voltage-switching (ZVS) intermediate voltage rails for CPU power supply. This approach combines a switched-capacitor stage to split the input voltage into multiple switched voltage rails, along with a multiphase buck stage connected in parallel at the output terminal. The proposed topology improves the utilization rate of components. It integrates flying capacitors as input filters for the buck stage and reuses switches for both two stages, thus enhancing power density. An LC network controls the slew rate of each intermediate voltage rail and enables ZVS of the switched-capacitor stage. Moreover, this design is scalable to a wide range of input voltages and output currents. The operational principle of this topology is introduced, and a 1-MHz/2-rail-2-phase prototype for 12-V-to-1-V conversion is built to verify the design's performance. The peak efficiency is 91.5% at 30 A and the full-power efficiency is 85.7% at 80 A.**

***Index Terms*—switched capacitor, voltage regulator module, zero voltage switching**

I. Introduction

Modern microprocessor systems necessitate lower operating voltages (below 1.85 V), higher load currents, and high slew rates to enhance processing speed, efficiency, and reliability [1]. These demands necessitate voltage regulation modules (VRMs) with rapid transient responses, entailing power conversion at higher switching frequencies (above 1 MHz). Additionally, for elevated power levels, utilizing a 48-V distribution bus voltage proves more advantageous than a 12-V distribution bus voltage to minimize distribution losses. Thus, meeting these criteria requires novel high-performance VRM topologies and control strategies. Many 48-V-to-1-V VRM topologies have been proposed to achieve efficient high step-down ratio conversion. These encompass transformer-based designs [2]–[4], and hybrid-switched-capacitor (HSC) designs [5]–[9]. Notably, two-stage HSC solutions hold particular allure as they effectively integrate the merits of switched-capacitor converters, characterized by elevated efficiency and power density, with the advantages of multi-phase buck converters (DrMOS), known for their substantial control bandwidth.

Recent studies have also shown that it is feasible to use the HSC converter as a voltage regulator stage for lower device rating and switching loss [10], [11]. The front-end unregulated stage and the regulator stage of the HSC solutions can be further integrated by removing redundant switches [12]–[15]. As a result, large decoupling capacitors are not required and the converter becomes a quasi single-stage solution with identical switching frequency for all switches. On the other hand, the parasitic inductance in these quasi single-stage solutions could be higher due to more components in the commutation loops, which may lead to higher device stress and loss, especially at high frequency operation.

The paper proposed a HSC-VRM topology with Zero-Voltage-Switching (ZVS) intermediate voltage rails, which is evolved from the topology presented in [16]. The original topology utilizes a switched-capacitor stage to split the input voltage and generate multiple square-wave intermediate voltage rails. Each intermediate voltage rail drives a single-phase or multi-phase buck converter. Comparing to the stiff intermediate voltage bus, utilizing square-wave intermediate voltage rail can remove one redundant switch. Thereby, the component count and conduction loss could be reduced. However, this topology still suffers from the device stress and loss caused by high parasitic inductance in the switching loop [17].

In the topology proposed by this paper, an inductor-capacitor (LC) network is inserted between the intermediate voltage rails and the ground reference to control the slew rate of the square-wave voltage, create ZVS opportunity for the switched-capacitor stage, and help absorb the switching spikes. Furthermore, the LC network is bypassed from the main power loop and its conduction loss is low. This design also exhibits high scalability, as it allows for multiple rails and multiphase buck modules to accommodate corresponding input voltage and output current levels. Subsequently, the operational principle is introduced and a 12-V-to-1-V/80-A/1-MHz prototype with 2 rails and 2 phases is built to validate the performance of the proposed architecture.

II. General Topology Overview

Fig. 1 shows the general circuit of the HSC-VRM with N ZVS intermediate voltage rails and N single-phase buck converters (each rail drives one buck converter). The architecture of HSC-VRM family is previously proposed in [16]. In this work, LC network (marked in red) is added to control the slew rate of each intermediate voltage rail. Resonant inductor L_r charges and discharges the effective capacitance (including the resonant capacitor C_r and the output capacitance of multiple

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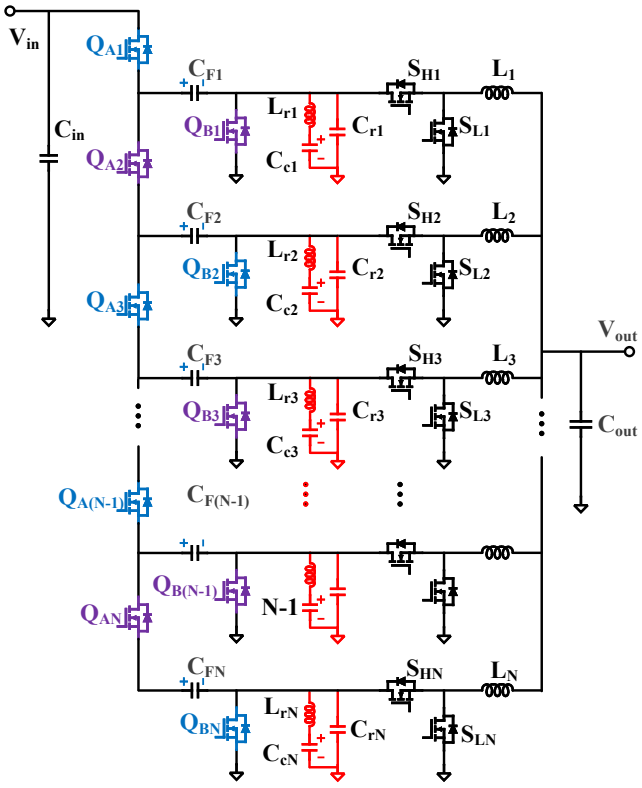


Fig. 1: The general circuit topology of the HSC-VRM with N ZVS intermediate voltage rails. Each rail drives a single-phase buck converter.

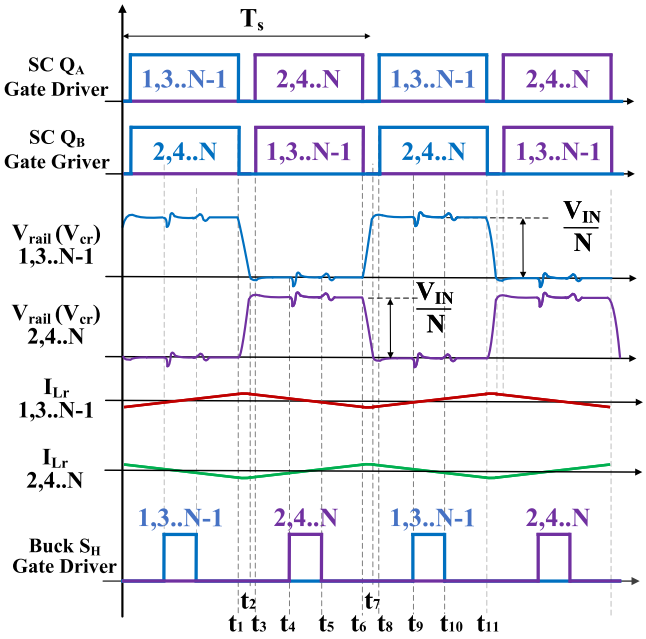


Fig. 2: The gate driver signals and theoretical voltage and current waveforms of the proposed HSC-VRM with N ZVS intermediate voltage rails and N phases buck converters.

switches) of each intermediate voltage rail. The charging and discharging time could be adjusted by the inductance of L_r and capacitance of C_r. Clamping capacitor C_c is relatively large for resetting L_r. Furthermore, one intermediate voltage rail with one LC network can drive a multi-phase buck converter.

The switches of the switched-capacitor stage can be divided into two groups: high-side floating switches (Q_A) and low-side grounded switches (Q_B). The gate driver signals of Q_A and Q_B exhibit complementary 50% square waves for every two adjacent switches. The dead-time of the switched-capacitor stage is longer than the charging and discharging time of the intermediate voltage rails for ZVS. Similar to the original topology in [16], the buck stage only switches when the rail voltage is not zero. And the low-side buck switch S_L is ZVS and the high-side buck switch S_H is still hard-switching. In addition, the existence of C_r helps absorb the switching spikes.

III. General Operational Principle

The gate driver signals and theoretical voltage and current waveforms of the proposed converter is given in Fig. 2. For balanced output current in each operation status, we assume N is an even number. The derivation of flying capacitor voltages is similar to other switched-capacitor topologies and can be directly given:

$$V_{CFi} = \frac{N-i}{N} V_{in}. \tag{1}$$

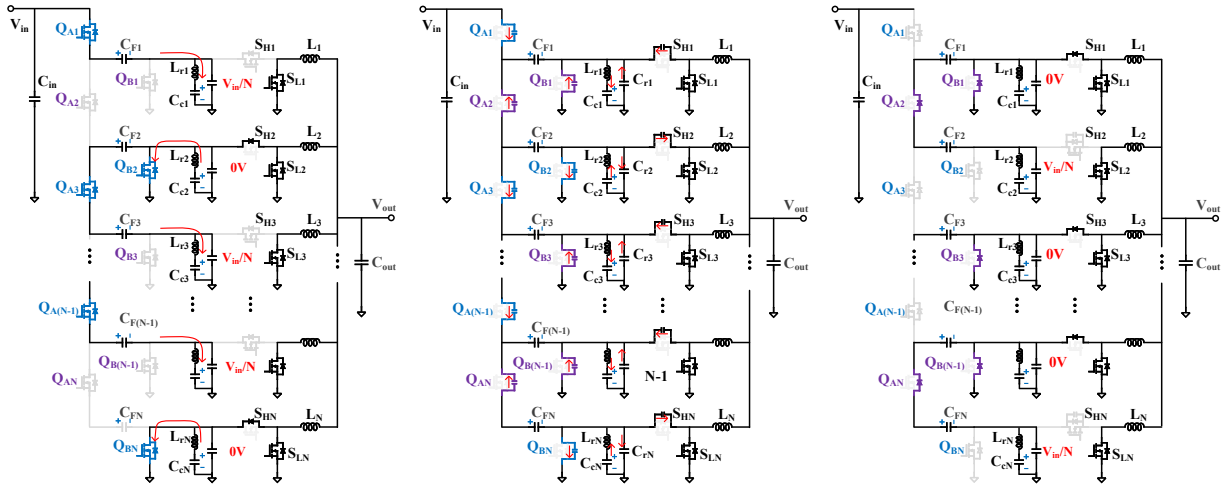
And the amplitude of each voltage rail is 0 and $\frac{V_{in}}{N}$. Notably, the voltage of the last flying capacitor V_{CFN} is 0. Thereby, Q_{AN}, Q_{BN} and the last LC network may be not required.

A. Operational Status

We assume all the C_F, L_r, L_r and C_c are the same, respectively. The operational status of the proposed topology in one switching cycle is shown in Fig. 3 and Fig. 4:

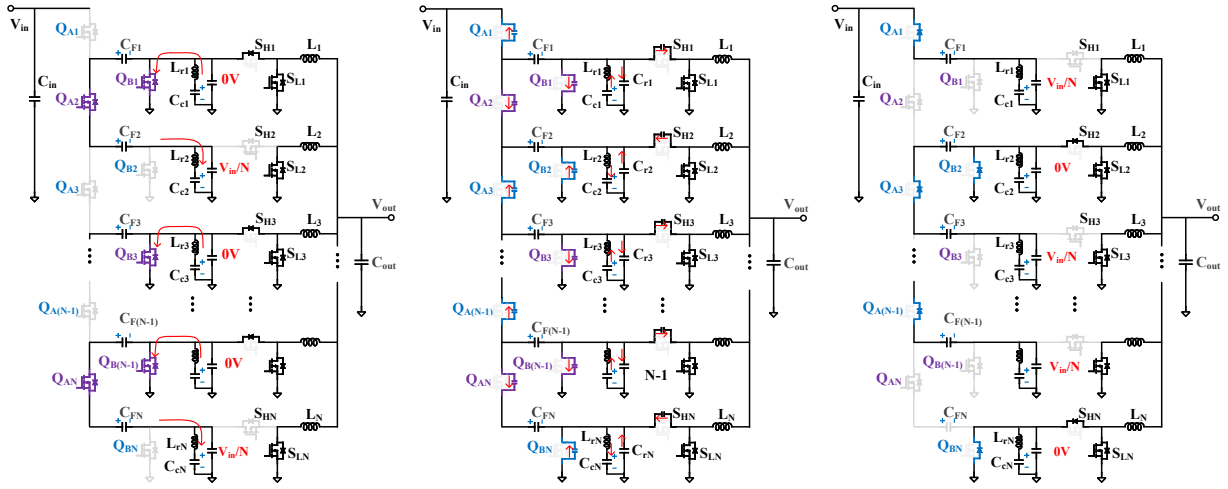
1) Before t_1, the voltage of the odd number rail is $\frac{V_{in}}{N}$ and the voltage of the even number rail is 0. All buck converters are freewheeling. L_{r1}, L_{r3}, ... $L_{r(N-1)}$ are charged by $\frac{V_{in}}{N} - V_{cc}$ and L_{r2}, L_{r4}, ... L_{rN} are reversely charged by $-V_{cc}$.
2) At t_1, Q_{A1}, Q_{A3}, ... $Q_{A(N-1)}$ and Q_{B2}, Q_{B4}, ... Q_{BN} are turned off by the same gate driver signal. Subsequently, their output capacitance, as well as C_{r2}, C_{r4}, ... C_{rN} are charged by all resonant inductors. Meanwhile, the output capacitance of Q_{A2}, Q_{A4}, ... Q_{AN} and Q_{B1}, Q_{B3}, ... $Q_{B(N-1)}$, as well as C_{r1}, C_{r3}, ... $C_{r(N-1)}$ are discharged. In addition, the output capacitance of S_{H2}, S_{H4}, ... S_{HN} are charged and the output capacitance of S_{H1}, S_{H3}, ... $S_{H(N-1)}$ are discharged.
3) At t_2, the output capacitance of Q_{A2}, Q_{A4}, ... Q_{AN} and Q_{B1}, Q_{B3}, ... $Q_{B(N-1)}$, as well as C_{r1}, C_{r3}, ... $C_{r(N-1)}$ are discharged to zero. The corresponding rail voltages V_{rail1}, V_{rail3}, ... $V_{rail(N-1)}$ are clamped to zero by the body-diodes of Q_{B1}, Q_{B3}, ... $Q_{B(N-1)}$. L_{r1}, L_{r3}, ... $L_{r(N-1)}$ begin to be reversely charged by $-V_{cc}$, and L_{r2}, L_{r4}, ... L_{rN} begin to be charged by

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(a) before t_1 (b) t_1 to t_2 (c) t_2 to t_3

Fig. 3: Operational status from t_1 to t_3.



(a) t_5 to t_6 (b) t_6 to t_7 (c) t_7 to t_8

Fig. 4: Operational status from t_5 to t_8.

$\frac{V_{in}}{N} - V_{cc}$. At t_3, Q_{A2}, Q_{A4}, … Q_{AN} and Q_{B1}, Q_{B3}, … $Q_{B(N-1)}$ are ZVS turned on by the same gate driver signal.

4) From t_3 to t_6, the operational status of the switched-capacitor stage remains unchanged. The buck converters driven by $V_{rail1}, V_{rail3}, \ldots V_{rail(N-1)}$ keep freewheeling and the remaining buck converters perform the commutation between the high-side switch and the low-side switch.
5) From t_6 to t_7, the operation is opposite to the operation from t_1 to t_2. The rail voltages V_{rail1}, V_{rail3}, … $V_{rail(N-1)}$ are charged from 0 to $\frac{V_{in}}{N}$, meanwhile the rail voltages V_{rail2}, V_{rail4}, … V_{railN} are discharged in the reverse direction.
6) At t_7, the rail voltages V_{rail2}, V_{rail4}, … V_{railN} are discharged to 0. The body-diodes of Q_{A1}, Q_{A3}, … $Q_{A(N-1)}$ and Q_{B2}, Q_{B4}, … Q_{BN} start to conduct and enable ZVS for the corresponding switches.

B. Component Voltage Stress

Notably, all the buck converters only switch when $V_{rail} = \frac{V_{in}}{N}$. Thereby, the steady-state voltage stress of the buck switches is $\frac{V_{in}}{N}$, which is the same as the voltage stress of the low-side grounded switches (Q_B) of the switched-capacitor stage. The steady-state voltage stress of the high-side floating switches is $\frac{2V_{in}}{N}$, except the top high-side switch Q_{A1}, which is still $\frac{V_{in}}{N}$.

The charging and discharging of the intermediate voltage rails are the resonance between the resonant inductors and the equivalent capacitance of each rail. The resonance must finish within the dead-time to ensure ZVS of the switched-capacitor stage. We assume the dead-time is short, e.g., 10% of

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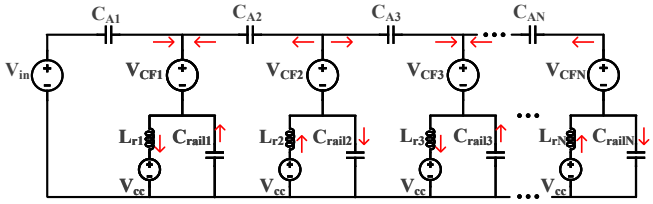


Fig. 5: The equivalent resonant circuit from t_1 to t_2.

the switching cycle. Thereby, the resonant inductor is linearly charged and discharged for the most of the switching cycle. In order to guarantee the charge balance of each resonant inductor, the voltage of each clamping capacitor must satisfy:

$$\frac{V_{in}}{N} - V_{cc} = V_{cc}. \tag{2}$$

That is, the steady-state voltage of each clamping capacitor is the half of the rail voltage amplitude $\frac{V_{in}}{2N}$.

C. Resonance Analysis

The resonance between the resonant inductors and the equivalent rail capacitance is relatively complicated because all of them are coupled. The equivalent resonant circuit from t_1 to t_2 is illustrated in Fig. 5, in which C_A represents the output capacitance of the high-side switches of the switched-capacitor stage, C_{rail} is the sum of the C_B (output capacitance of the low-side switch Q_B), C_r and C_H (output capacitance of the high-side buck switch S_H) of each voltage rail. The resonant equations of each voltage rails can be obtained:

$$\begin{cases} L_r \frac{\mathrm{d}i_{Lr}}{\mathrm{d}t} + V_{cc} = V_{rail} \\ C_{eq} \frac{\mathrm{d}v_{rail}}{\mathrm{d}t} = -i_{Lr} \end{cases} \tag{3}$$

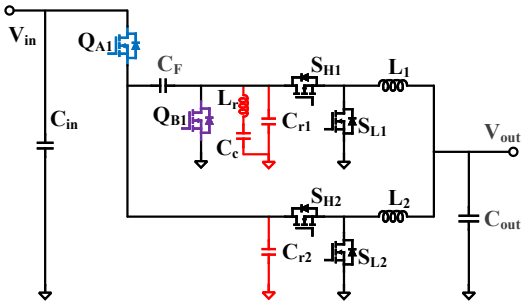
where C_{eq} represents the combined equivalent capacitance needed for resonance, and its value is determined by the circuit structure of each individual node. $C_{eq} = C_{rail} + 4C_A$ when $1 < n < N-1$. For the first and the last rail, $C_{eq} = C_{rail} + 3C_A$.

The initial value of v_{rail1}, v_{rail3}, v_{rail5} ... at t_1 is $\frac{V_{in}}{N}$, and initial value of the remaining rail voltages is 0. We assume the inductance of L_r is relatively high and its current changes slightly during the resonance. Thereby, the initial value of resonant inductor current could be estimated by

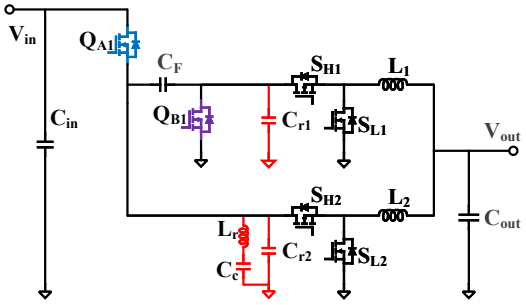
$$\begin{cases} i_{Lr,1,3,5\ldots}|_{t=t_1} = \frac{V_{in}T_s}{8NL_r} \\ i_{Lr,2,4,6\ldots}|_{t=t_1} = -\frac{V_{in}T_s}{8NL_r} \end{cases} \tag{4}$$

Solve (3) with the initial conditions, the time domain expression of each voltage rail starting from t_1 is given by (5).

$$\begin{cases} v_{rail,1,3,5\ldots} = \frac{V_{in}}{2N}\cos(\omega_r t) - \frac{V_{in}\omega_r}{8Nf_s}\sin(\omega_r t) + \frac{V_{in}}{2N} \\ v_{rail,2,4,6\ldots} = -\frac{V_{in}}{2N}\cos(\omega_r t) + \frac{V_{in}\omega_r}{8Nf_s}\sin(\omega_r t) + \frac{V_{in}}{2N} \end{cases} \tag{5}$$



(a) Resonant inductor at the top rail, $V_{cc} = \frac{V_{in}}{4}$



(b) Resonant inductor at the bottom rail, $V_{cc} = \frac{3V_{in}}{4}$

Fig. 6: Two embodiments of the HSC-VRM with 2 ZVS intermediate voltage rails.

where $\omega_r = \frac{1}{\sqrt{LrC_{eq}}}$ is the resonant frequency. The time of fully discharging $v_{rail,1,3,5\ldots}$ to 0 is given by (6) ,

$$T_{fall} = \frac{1}{\omega_r}\left(\arcsin\frac{1}{\sqrt{\frac{\omega_r^2}{16f_s^2}+1}} + \arctan\frac{4f_s}{\omega_r}\right) \tag{6}$$

For the second resonance from t_6 to t_7, the equivalent resonant circuit is the same and all voltages and currents changes in the opposite direction. (6) is still valid for calculating the time of fully discharging $v_{rail,2,4,6\ldots}$.

IV. Case with 2 ZVS Intermediate Rails

Generally, N intermediate voltage rails require N groups of Q_A and Q_B with C_F in the switched-capacitor stage. The analysis in Section III also shows that the voltage of the bottom C_F is 0 and the corresponding switched-capacitor switches could be removed. This indicates that only one group of Q_A and Q_B with C_F are required for two intermediate voltage rails. The circuit topologies of the 2-Rail case are shown in Fig. 6. The resonant inductor and the clamping capacitor can be either installed at the top rail or the bottom rail.

The gate driver signals and theoretical voltage and current waveforms of the proposed converter with 2 ZVS intermediate voltage rails is given in Fig. 7. The amplitudes of V_{rail2} (the bottom rail) are V_{in} and $\frac{V_{in}}{2}$ after removing Q_{A2}, Q_{B2} and C_{F2}. Two buck converters still switch when $V_{rail1} = \frac{V_{in}}{2}$ and $V_{rail2} = \frac{V_{in}}{2}$, whereas the steady-state voltage stress of S_{H2} increases to V_{in}. The average voltage of C_c is $\frac{3V_{in}}{4}$ when L_r and C_c are installed at the bottom rail.

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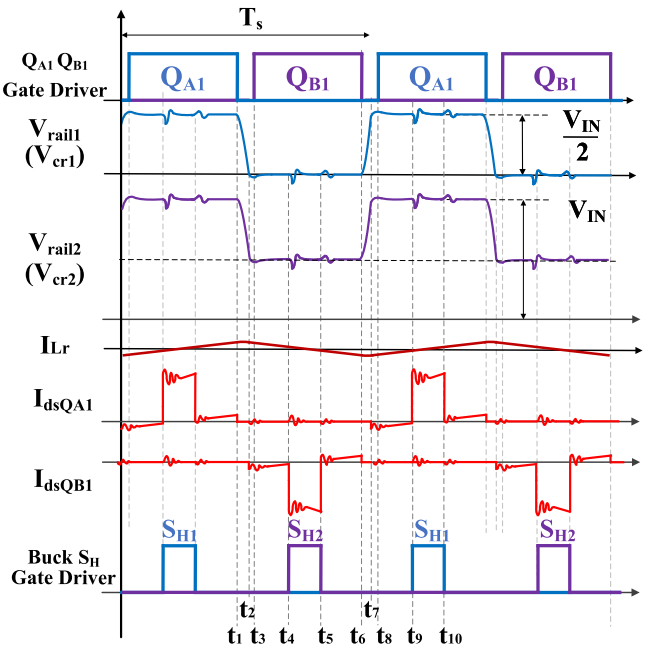


Fig. 7: The gate driver signals and theoretical voltage and current waveforms of the proposed HSC-VRM with 2 ZVS intermediate voltage rails and 2 phases of buck converters.

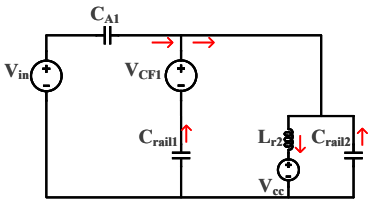


Fig. 8: The equivalent resonant circuit of the 2-Rail HSC-VRM from t_1 to t_2.

Notably, the drain-source currents of Q_{A1} and Q_{B1} are the superposition of the drain-source currents of high-side buck switches and the resonant inductor current. Q_{A1} and Q_{B1} could be Zero-Current-Switching (ZCS) without the LC network in the original topology [16]. However, ZCS is more suitable for minority-carrier semiconductor devices like IGBT and turn-on loss still exists with ZCS. ZVS is preferable for MOSFETs, which are more commonly used in low-voltage high-current VRM applications. On the other hand, the resonant inductor current could increase the conduction loss of Q_{A1} and Q_{B1}. Thereby, the inductance of L_r is critical to both ZVS and conduction loss.

The equivalent resonant circuit with 2 rails from t_1 to t_2 is illustrated in Fig. 8. The resonant equations are the same as (3) and the equivalent capacitance $C_{eq} = C_A + C_{rail1} + C_{rail2}$, where $C_{rail1} = C_{B1} + C_{H1} + C_{r1}$ and $C_{rail2} = C_{H2} + C_{r2}$.

TABLE I: BOM of the 12-V-to-1-V/2-Rail Prototype

Q_A, Q_B	BSZ011NE2LS5I: 25 V, 1.1 mΩ
S_H, S_L	TDA21490, V_{max} = 25 V, I_{max} = 70 A
C_F	10-V/0805/X7S MLCC ×3, $C_{eff.}$ = 16.5 µF
L_{out}	FP0805R1-R10-R,100 nH/50 A/DCR = 0.17 mΩ
Gate Driver	Half-bridge UCC27284DRMR ×1
L_r	LPS4018-561, 560 nH/4.8 A/DCR = 33 mΩ
C_r	C0G/1 nF MLCC ×6, $C_{eff.}$ = 6 nF
C_c	16-V/0805/X7S MLCC ×4, $C_{eff.}$ = 20 µF

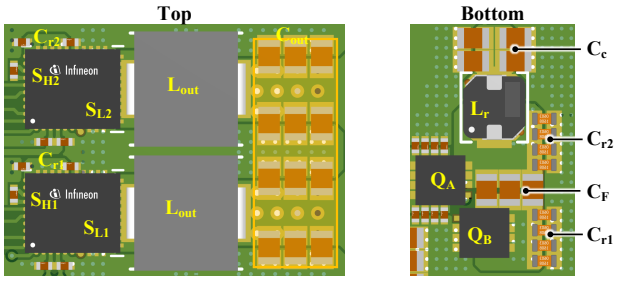


Fig. 9: The double-sided PCB layout design for the 12-V-to-1-V/2-Rail Prototype.

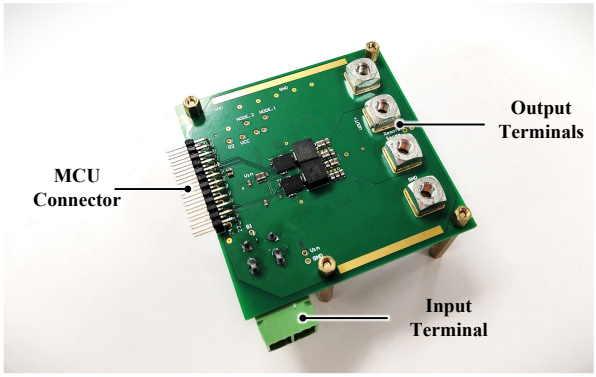


Fig. 10: The photo of the 12-V-to-1-V/2-Rail Prototype.

V. Prototype Design

This section introduces the prototype design of a 12-V-to-1-V HSC-VRM with 2 ZVS intermediate voltage rails and 2 phases of buck converters. The LC network is installed at the bottom rail as Fig. 6(b). The bill-of-materials of the prototype are listed in Table I. We use discrete MOSFET as Q_A and Q_B and use DrMOS as the buck stage. DrMOS has integrated gate driver and automatically adjusted dead-time with a 5×6 mm footprint. Thereby only one half-bridge gate driver Ic is needed for Q_A and Q_B. The gate driver configuration for Q_A and Q_B is the same as the original topology proposed in [16]. That is, the gate driver of Q_B is powered by the 5-V auxiliary power supply and the gate driver of Q_A is bootstrapped from V_{in} with a V_{DD} at $V_{in} - V_{CF} = 6$ V.

All MOSFETs have a steady-state voltage stress of 6V, except for S_{H2}, which has a stress of 12V. The current ripple

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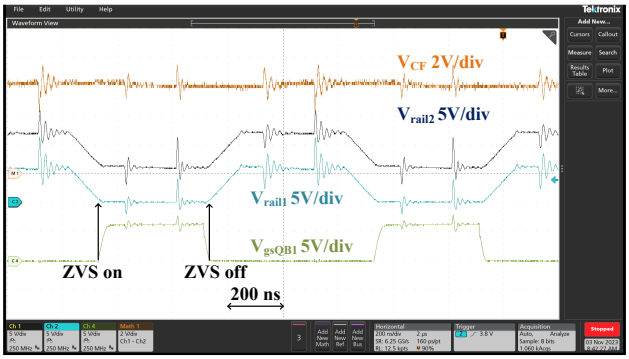


Fig. 11: The flying capacitor voltage, two ZVS rail voltages and the gate driver voltage of Q_{B1}, with L_r, C_r and C_c installed. $I_{out} = 50$ A, $f_s = 1$ MHz.

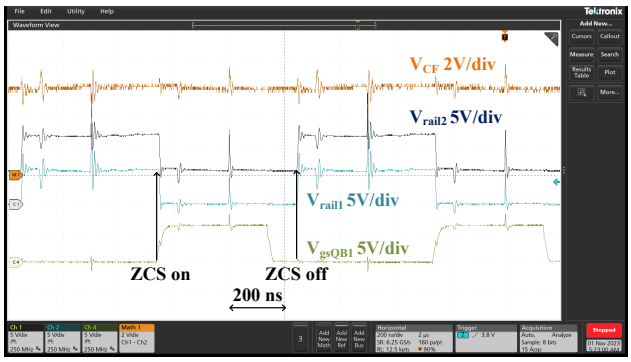
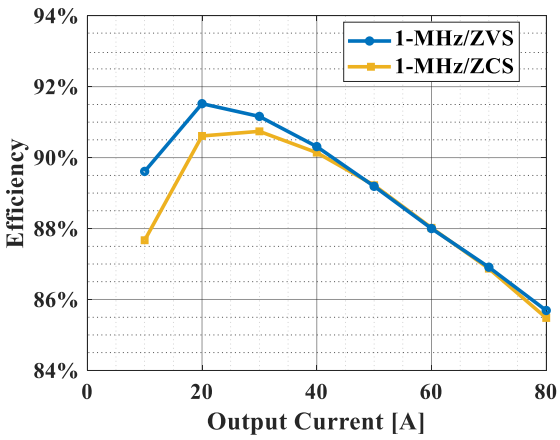


Fig. 12: The flying capacitor voltage, two square-wave rail voltages and the gate driver voltage of Q_{B1}, without L_r, C_r and C_c. $I_{out} = 50$ A, $f_s = 1$ MHz.

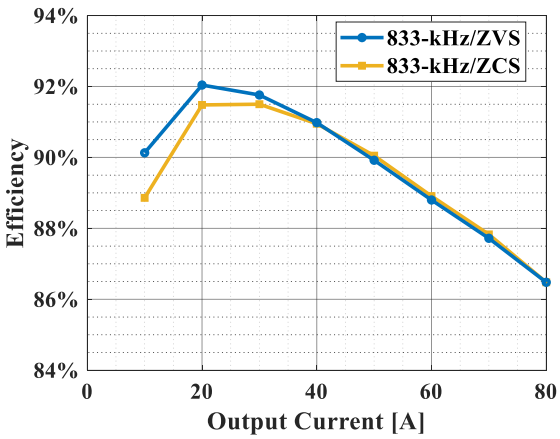
of the buck stage inductor can be expressed as $\Delta I_{ph} = \frac{V_{out}(1-D)}{f_s L_{out}}$, where D is the steady-state duty cycle of each buck phase and f_s is the switching frequency. $\Delta I_{ph} = 8.33$ A at 1 MHz $L_{out} = 100$ nH. Meanwhile, the flying capacitance can be calculated by $C_F = \frac{I_{ph} D T_s}{\Delta V}$, where ΔV is the tolerated voltage ripple of the flying capacitor C_F, and I_{PH} is the output current of each buck converter. Considering $I_{out} = 2I_{PH} = 80$ A, $\Delta V \leq 2$ V with $C_F = 16.5$ µF. X7S MLCC capacitors with low ESR are selected.

The resonant inductor current is almost a triangle wave and the amplitude can be calculated by (4), which is 1.34 A with $L_r = 560$ nH and $f_s = 1$ MHz. The output capacitance of Q_A and Q_B is nonlinear and its value is around 2 nF to 4 nF with V_{ds} from 0 V to 6 V. The output capacitance of DrMOS is undisclosed. Thereby, we assume $C_A = C_B = 3$ nF and $C_H = 0.75$ nF. Together with $C_r = 6$ nF, the resonant time is 125 ns.

The PCB layout design for the 12-V-to-1-V/2-Rail Prototype is shown in Fig. 9. Two buck converters (DrMOS) are placed on the top side. The switched-capacitor stage and the LC network are placed on the bottom side. Fig. 10 is the photo of the 12-V-to-1-V/2-Rail Prototype. The gate driver signals are generated by TMS320F28388D real-time microcontroller.



(a) 12-V-to-1-V/1-MHz



(b) 12-V-to-1-V/833-kHz

Fig. 13: Measured efficiency of the 12-V-to-1-V/2-Rail Prototype. ZVS: with L_r, C_r and C_c; ZCS: without L_r, C_r and C_c.

VI. Experiment Results

Fig. 11 displays the waveforms of flying capacitor voltage, two ZVS rail voltages and the gate driver voltage of Q_{B1}, with L_r, C_r and C_c installed. The input voltage is 12 V, the output voltage is 1 V, $I_{out} = 50$ A, $f_s = 1$ MHz. Both the rise time and the fall time of the intermediate voltage rails are around 125 ns. The gate driver voltage of Q_{B1} rises after V_{rail1} is discharged to 0, which means Q_{B1} is ZVS turned-on. Similarly, Q_{A1} is ZVS turned-on when V_{rail2} is charged to V_{in}. Fig. 12 shows the same waveforms without L_r, C_r and C_c. V_{rail1} and V_{rail2} become square wave. Even through Q_{A1} and Q_{B1} are ZCS, the dissipation of the energy stored in their output capacitance still causes switching loss and voltage spikes. Furthermore, the commutation of the buck stage induces high voltage spikes on two voltage rails. With C_r installed, the voltage spike is partially absorbed and the peak voltage is reduced.

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Fig. 14: The thermal image of the prototype at 12-V-to-1-V/80-A/1-MHz.

Fig. 13 shows the measured efficiency of the 12-V-to-1-V/2-rail prototype, including the loss of the power stage and the gate driver loss of Q_{A1}. The switched-capacitor stage are ZVS with L_r, C_r and C_c, and ZCS without L_r, C_r and C_c. The peak efficiency is 91.5% at 20 A and the full-load efficiency at 80 A is around 85.7% at 1 MHz with ZVS. The light-load efficiency is 2% lower and the peak-efficiency is 1% lower with ZCS. At 833-kHz, the efficiency gap between ZVS and ZCS narrows because the portion of the switching loss of the switched-capacitor stage in the overall loss decreases. Another reason is that with longer switching cycle, the peak current of L_r as well as the inductor loss increase.

Fig. 14 is the thermal image of this prototype working at 12-V-to-1-V/80-A/1-MHz. The testing is performed with a single fan cooling and the ambient temperature is 25°C. The hot spot locates near the high-side switch of DrMOS and the resonant capacitors close to DrMOS. The maximum temperature is 66°C.

VII. Conclusions

This paper proposes a HSC-VRM topology with ZVS intermediate voltage rails, incorporating a SC stage with a scalable buck stage. This design optimizes device utilization, reducing components in each rail and improving scalability. A 12-V-to-1-V/1-MHz prototype is built to validate the proposed topology's performance. With the LC network, the switched-capacitor stage achieves ZVS. The light-load efficiency and peak-efficiency are improved by 2% and 1% comparing the the original solution with a ZCS switched-capacitor stage.

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